ADDENDUM PAGES

8. (Twice Amended) The circuit employed in [a]the receiver of Claim 7, wherein said continuous time commutator comprises:

a complementary amplifier configured to receive said incoming signal and to produce an inverted version of said incoming signal at an inverted output port and to produce a non-inverted version of said incoming signal at a non-inverted output port; and

a switch having a first input port coupled to said inverted output port, having a second input port coupled to said non-inverted output port and having a control port coupled to said digital conversion clock.

9. (Twice Amended) The circuit employed in [a]the receiver of Claim 7, wherein said delta-sigma modulator comprises:

a loop amplifier having a first input port coupled to said output port of said continuous time modulator, having a second input, and having an output port;

a continuous time loop filter coupled to said output port of said loop amplifier and having an output port;

an edge-triggered comparator coupled to said output port of continuous time loop filter, having a clock input coupled to said digital conversion clock and having an output port; and

a one-bit digital to analog converter having an input port coupled to said output port of said edge-triggered comparator and having an output port coupled to said second input of said loop amplifier.

10. (Twice Amended) The circuit employed in [a]the receiver of claim 7, further comprising a programmable digital filter having an input port coupled to said output of said delta-sigma modulator, said programmable digital filter configured to filter said series of digital

values according a filter characteristics selected based upon a type of modulation of said modulation waveform.

11. (Twice Amended) The circuit employed in [a]the receiver of claim 7, further comprising an antenna coupled to said continuous time commutator so as to receive said incoming signal, wherein an amplitude of said incoming signal is in fixed proportion to an amplitude of a signal strength received by said antenna.

12. (Twice Amended) The circuit employed in [a]the receiver of claim 7, further comprising a filter configured to receive an antenna signal and configured to prevent aliasing of out-of-band signal and noise power into a desired signal band, said filter coupled to said input port of said continuous time commutator, wherein a frequency of said conversion clock is selected from a range of frequencies passed by said filter.

17. (Twice Amended) The apparatus of claim 14, wherein said means for inverting [performs the steps of]comprises:

means for producing an inverted signal representation of said incoming waveform;

means for producing a non-inverted signal representation of said incoming waveform;

means for coupling said inverted signal representation to a first input port of a switch;

means for coupling said non-inverted signal representation to a second input port of said switch; and

means for coupling said conversion clock to a control port of said switch.